IN THE CLAIMS:

Claims 4, 5, 27, 42, 44, and 64 were previously cancelled. Claims 16-18, 20-22, 25, 28, 29, 31-37, 43, 58-60, 62, 63, 66-72, 80, 82, 83, 86-92, 100, 102, 103, and 106-108 have been amended herein. All of the pending claims are presented below. This listing of claims will replace all prior versions and listings of claims in the application. Please enter these claims as amended.

1. (Previously presented) An integrated circuit manufacturing process using data related to manufacturing procedures used previously that a plurality of integrated circuits of Dynamic Random Access Memory (DRAM) semiconductor devices have undergone for selecting manufacturing procedures the plurality of integrated circuits of the Dynamic Random Access Memory (DRAM) semiconductor devices are to undergo, each Dynamic Random Access Memory (DRAM) semiconductor device having integrated circuits and having a substantially unique identification code, the manufacturing process comprising:

storing data in association with the identification code of each Dynamic Random Access Memory (DRAM) semiconductor device of the plurality identifying manufacturing procedures each Dynamic Random Access Memory (DRAM) semiconductor device has undergone, said storing data comprising storing data that identifies spare rows and columns used in repairing each DRAM semiconductor device;

automatically reading the identification code of each Dynamic Random Access Memory (DRAM) semiconductor device; and

accessing the data stored in association with the identification code of each Dynamic Random Access Memory (DRAM) semiconductor device.

2. (Original) The process of claim 1, further comprising:

selecting manufacturing procedures each semiconductor device undergoes in accordance with the accessed data.

3. (Previously presented) The process of claim 1, wherein storing data comprises storing data that identifies repairs performed on each semiconductor device.

4. (Cancelled)

5. (Cancelled)

6. (Previously presented) The process of claim 1, wherein storing data comprises storing data at probe.

7. (Previously presented) The process of claim 1, wherein automatically reading the identification code of each semiconductor device comprises electrically retrieving a unique fuse ID programmed into each semiconductor device.

8. (Previously presented) The process of claim 1, wherein automatically reading the identification code of each semiconductor device comprises optically reading a unique ID code provided on each semiconductor device.

9. (Previously presented) The process of claim 8, wherein optically reading a unique ID code provided on each semiconductor device comprises optically reading a unique laser fuse ID programmed into each semiconductor device.

10. (Previously presented) The process of claim 1, wherein automatically reading the identification code of each semiconductor device comprises automatically reading the identification code of each semiconductor device at one of an opens/shorts test, a burn-in test, and a back-end test in the integrated circuit manufacturing process.

11. (Previously presented) The process of claim 1, wherein accessing the data stored in association with the identification code of each semiconductor device comprises accessing the data stored in association with the identification code of each semiconductor device at one of an opens/shorts test, a burn-in test, and a back-end test in the integrated circuit manufacturing process.

12. (Previously presented) The process of claim 2, wherein selecting the manufacturing procedures each semiconductor device undergoes in accordance with the accessed data comprises selecting repairs each semiconductor device undergoes in accordance with the accessed data.

13. (Previously presented) The process of claim 12, wherein each semiconductor device comprises Dynamic Random Access Memory (DRAM) semiconductor device, wherein selecting repairs each semiconductor device undergoes comprises selecting spare rows and columns used to repair each DRAM semiconductor device.

14. (Previously presented) The process of claim 2, wherein selecting manufacturing procedures each semiconductor device undergoes in accordance with the accessed data comprises selecting whether each semiconductor device undergoes repair procedures.

15. (Previously presented) The process of claim 14, wherein each semiconductor device comprises a Dynamic Random Access Memory (DRAM) semiconductor device, and wherein selecting whether each semiconductor device undergoes repair procedures comprises selecting whether each DRAM semiconductor device will be repaired in accordance with whether the accessed data indicates enough spare rows and columns are available in each semiconductor device to effect repairs.

16. (Currently amended) The process of claim 2, wherein selecting manufacturing procedures each semiconductor device will undergo in accordance with the accessed data comprises determining whether each semiconductor device will be assembled into Multi-Chip Modules ~~(MCM's)~~ (MCMs) in accordance with whether the accessed data indicates each semiconductor device is repairable.

17. (Currently amended) The process of claim 1, further comprising assembling each semiconductor device into a packaged semiconductor device after ~~the step of~~ storing data and before ~~the step of~~ automatically reading the identification code of each semiconductor device.

18. (Currently amended) A method of manufacturing integrated circuit Dynamic Random Access Memory (DRAM) semiconductor devices from semiconductor wafers, the method comprising:

providing a plurality of semiconductor wafers;

fabricating a plurality of Dynamic Random Access Memory (DRAM) semiconductor devices on each of the semiconductor wafers of the plurality of semiconductor wafers;

causing each Dynamic Random Access Memory (DRAM) semiconductor device of the plurality on each of the semiconductor wafers of the plurality of semiconductor wafers to store a substantially unique identification code;

storing data in association with the identification code of each Dynamic Random Access Memory (DRAM) semiconductor device of the plurality that identifies manufacturing procedures each Dynamic Random Access Memory (DRAM) semiconductor device of the plurality has undergone, said storing data comprising storing data that identifies spare rows and columns used in repairing each DRAM semiconductor device of the plurality;

separating each Dynamic Random Access Memory (DRAM) semiconductor device of the plurality on each of the semiconductor wafers of the plurality of semiconductor wafers from its wafer to form one Dynamic Random Access Memory (DRAM) semiconductor

device of a plurality of Dynamic Random Access Memory (DRAM) semiconductor devices;

assembling each Dynamic Random Access Memory (DRAM) semiconductor device of the plurality into a Dynamic Random Access Memory (DRAM) semiconductor device assembly;

automatically reading the identification code associated with each Dynamic Random Access Memory (DRAM) semiconductor device of the plurality; and

accessing the data stored in association with the identification code associated with each Dynamic Random Access Memory (DRAM) semiconductor device of the plurality.

19. (Previously presented) The method of claim 18, further comprising:

selecting manufacturing procedures each semiconductor device undergoes in accordance with the accessed data.

20. (Currently amended) The method of claim 18, wherein fabricating a plurality of semiconductor devices on each of the semiconductor wafers of the plurality of semiconductor wafers comprises fabricating semiconductor devices selected from a group comprising Dynamic Random Access Memory (DRAM) semiconductor devices, Static Random Access Memory (SRAM) semiconductor devices, Synchronous DRAM (SDRAM) semiconductor devices, processor semiconductor devices, Rambus in-line memory module type semiconductor devices, small outline Rambus in-line memory module type semiconductor devices, and personal computer memory format type semiconductor devices.

21. (Currently amended) The method of claim 18, wherein causing each semiconductor device on each of the semiconductor wafers of the plurality of semiconductor wafers to store a substantially unique identification code comprises programming each semiconductor device on each of the semiconductor wafers of the plurality of semiconductor wafers to permanently store a unique fuse ID.

22. (Currently amended) The method of claim 21, wherein programming each semiconductor device on each of the semiconductor wafers of the plurality of semiconductor wafers to permanently store a unique fuse ID comprises programming at least one of fuses and anti-fuses in each semiconductor device on each of the semiconductor wafers of the plurality of semiconductor wafers to permanently store a unique fuse identification.

23. (Previously presented) The method of claim 18, wherein assembling each semiconductor device of the semiconductor devices into a semiconductor device assembly comprises:

picking each semiconductor device from its wafer;

placing each semiconductor device onto an epoxy-coated bonding site of one lead frame of a plurality of lead frames;

curing the epoxy on the bonding site of each lead frame of the lead frames;

wire bonding each semiconductor device to its associated lead frame;

encapsulating each semiconductor device and its associated lead frame to form one of a plurality of semiconductor device assembly packages, each package having projecting leads;

curing each of the semiconductor device assembly packages;

de-flashing the projecting leads of each semiconductor device assembly package;

electroplating the projecting leads of each semiconductor device assembly package; and

singulating each semiconductor device assembly package into one semiconductor device assembly package of a plurality of discrete semiconductor device assembly packages.

24. (Previously presented) The method of claim 18, wherein assembling each semiconductor device into a semiconductor device assembly comprises assembling each semiconductor device into a semiconductor device assembly selected from a group comprising a wire bond/lead frame semiconductor device, a Chip-On-Board (COB) semiconductor device, a flip-chip semiconductor device, and a Board-Over-Chip (BOC) semiconductor device.

25. (Currently amended) A method of manufacturing Multi-Chip Modules ~~(MCM's)~~ (MCMs) from semiconductor wafers, the ~~MCM's~~ MCMs selected from a group of Single In-Line Memory Modules ~~(SIMM's)~~ (SIMMs) and Dual In-line Memory Modules ~~(DIMM's),~~ (DIMMs), Rambus In-Line Memory Modules ~~(RIMM),~~ (RIMMs), Small Outline Rambus In-Line Memory Modules ~~(SO-RIMM),~~ (SO-RIMMs), Personal Computer Memory Format (PCMCIA), and Board-Over-Chip type substrates, the method comprising:

providing a plurality of semiconductor wafers;

fabricating a plurality of semiconductor devices on each of the semiconductor wafers of the plurality of semiconductor wafers;

causing each semiconductor device of the plurality of semiconductor devices on each of the semiconductor wafers of the plurality of semiconductor wafers to store a substantially unique identification code;

storing data in association with the identification code of each semiconductor device of the semiconductor devices that identifies manufacturing procedures each semiconductor device of the plurality of semiconductor devices has undergone, said storing data including storing data that identifies rows and columns used in repairing a semiconductor device;

separating each semiconductor device of the plurality of semiconductor devices on each semiconductor wafer of the plurality of semiconductor wafers from its wafer to form one semiconductor device of a plurality of semiconductor devices;

assembling one or more of the semiconductor devices of the plurality into each of a plurality of ~~MCM's;~~ MCMs;

automatically reading the identification code of each semiconductor device of the plurality of semiconductor devices in each MCM of the plurality of ~~MCM's;~~ MCMs; and

accessing the data stored in association with the identification code of each semiconductor device of the plurality of semiconductor devices in each MCM of the plurality of ~~MCM's.~~ MCMs.

26. (Original) The method of claim 25, further comprising:

selecting manufacturing procedures the semiconductor devices will undergo in accordance with the accessed data.

27. (Cancelled)

28. (Currently amended) A method of manufacturing Dynamic Random Access Memory (DRAM) semiconductor devices from semiconductor wafers, the method comprising:

providing a plurality of semiconductor wafers;

fabricating a plurality of Dynamic Random Access Memory (DRAM) semiconductor devices on each semiconductor wafer of the plurality of semiconductor wafers;

electronically probing each Dynamic Random Access Memory (DRAM) semiconductor device of the plurality of Dynamic Random Access Memory (DRAM) semiconductor devices on each semiconductor wafer of the plurality of semiconductor wafers to identify good, bad and repairable semiconductor devices on each semiconductor wafer of the plurality of semiconductor wafers;

repairing the repairable Dynamic Random Access Memory (DRAM) semiconductor devices;

programming each Dynamic Random Access Memory (DRAM) semiconductor device of the plurality of Dynamic Random Access Memory (DRAM) semiconductor devices on each semiconductor wafer of the plurality of semiconductor wafers to store a unique fuse identification;

storing data in association with the fuse identification of each of the Dynamic Random Access Memory (DRAM) semiconductor devices identifying repairs performed on each Dynamic Random Access Memory (DRAM) semiconductor device of the plurality of Dynamic Random Access Memory (DRAM) semiconductor devices, said storing data comprising storing data that identifies spare rows and columns used in repairing each DRAM semiconductor device of the plurality;

mounting each semiconductor wafer of the plurality of semiconductor wafers on an adhesive film;

sawing each Dynamic Random Access Memory (DRAM) semiconductor device of the plurality of Dynamic Random Access Memory (DRAM) semiconductor devices on each semiconductor wafer of the plurality of semiconductor wafers from its wafer to form one of a plurality of discrete Dynamic Random Access Memory (DRAM) semiconductor devices;

automatically picking each Dynamic Random Access Memory (DRAM) semiconductor device of the plurality of Dynamic Random Access Memory (DRAM) semiconductor devices from its wafer;

placing each Dynamic Random Access Memory (DRAM) semiconductor device of the plurality of Dynamic Random Access Memory (DRAM) semiconductor devices onto an epoxy-coated bonding site of one lead frame of a plurality of lead frames;

curing the epoxy on the bonding site of each lead frame of the lead frames;

wire bonding each Dynamic Random Access Memory (DRAM) semiconductor device of the plurality of Dynamic Random Access Memory (DRAM) semiconductor devices to its associated lead frame;

encapsulating each Dynamic Random Access Memory (DRAM) semiconductor device of the plurality of Dynamic Random Access Memory (DRAM) semiconductor devices and its associated lead frame to form one of a plurality of Dynamic Random Access Memory (DRAM) semiconductor device assembly packages, each Dynamic Random Access Memory (DRAM) semiconductor device assembly package having projecting leads;

curing each Dynamic Random Access Memory (DRAM) semiconductor device assembly package;

de-flashing the projecting leads of each Dynamic Random Access Memory (DRAM) semiconductor device package;

electroplating the projecting leads of each Dynamic Random Access Memory (DRAM) semiconductor device package;

singulating each Dynamic Random Access Memory (DRAM) semiconductor device package;

testing each Dynamic Random Access Memory (DRAM) semiconductor device assembly package for opens and shorts;

burn-in testing each Dynamic Random Access Memory (DRAM) semiconductor device assembly package;

back-end testing each Dynamic Random Access Memory (DRAM) semiconductor device assembly package;

automatically reading an ID of each Dynamic Random Access Memory (DRAM) semiconductor device assembly package;

accessing data stored in association with the ID of each Dynamic Random Access Memory (DRAM) semiconductor device assembly package;

for any Dynamic Random Access Memory (DRAM) semiconductor device assembly package failing any one of the opens/shorts, burn-in, and back-end tests, evaluating the accessed data to determine whether the failing semiconductor device assembly package may be repaired;

repairing the Dynamic Random Access Memory (DRAM) semiconductor device assembly package determined in accordance with the accessed data to be repairable and returning the repaired Dynamic Random Access Memory (DRAM) semiconductor device assembly package to the semiconductor manufacturing process; and

discarding the Dynamic Random Access Memory (DRAM) semiconductor device assembly package determined in accordance with the accessed data to be unrepairable.

29. (Currently amended) The method of claim 28, wherein mounting the semiconductor wafers comprises mounting each semiconductor wafer of the plurality of semiconductor wafers on an ultraviolet (U.V.) adhesive film, wherein the method further comprises exposing the U.V. adhesive film to U.V. light to loosen the semiconductor wafers from the film prior to picking and placing each semiconductor device.

30. (Original) The method of claim 28, further comprising receiving a plurality of unrepairable semiconductor devices diverted from another semiconductor device manufacturing process.

31. (Currently amended) A method of manufacturing Multi-Chip Modules ~~(MCM's)~~ (MCMs) from semiconductor wafers using Chip-On-Board (COB) techniques, the method comprising:

providing a plurality of semiconductor wafers;

fabricating a plurality of semiconductor devices on each semiconductor wafer of the plurality of semiconductor wafers;

electronically probing each semiconductor device of the plurality of semiconductor devices on each semiconductor wafer of the plurality of semiconductor wafers to identify good, bad and repairable semiconductor devices on each semiconductor wafer of the plurality of semiconductor wafers;

repairing the repairable semiconductor devices;

programming each semiconductor device of the plurality of semiconductor devices on each semiconductor wafer of the plurality of semiconductor wafers to store a unique fuse identification;

storing an electronic wafer map for each semiconductor wafer of the plurality of semiconductor wafers that identifies locations of good and bad semiconductor devices on each semiconductor wafer of the plurality of semiconductor wafers and associates each semiconductor device on each semiconductor wafer of the plurality of semiconductor wafers with its fuse identification;

storing data in association with the fuse identification of each semiconductor device of the semiconductor devices identifying repairs performed on each semiconductor device of the plurality of semiconductor devices;

mounting each semiconductor wafer of the plurality of semiconductor wafers on an adhesive film;

sawing each semiconductor device of the plurality of semiconductor devices on each semiconductor wafer of the plurality of semiconductor wafers from its wafer to form one discrete semiconductor device;

accessing the stored wafer map for each semiconductor wafer of the plurality of semiconductor wafers;

accessing the stored data for each semiconductor device on each semiconductor wafer of the plurality of semiconductor wafers;

automatically picking each semiconductor device of the good semiconductor devices from its wafer;

discarding non-picked semiconductor devices identified as bad by the accessed wafer maps;

diverting picked semiconductor devices identified as good but unrepairable by the accessed wafer maps and data to a non-MCM semiconductor manufacturing process;

placing picked semiconductor devices identified as good and repairable by the accessed wafer maps and data onto epoxy-coated bonding sites of a plurality of printed circuit boards using COB techniques to form a plurality of ~~MCM's;~~ MCMs;

curing the epoxy on the bonding sites of each MCM of the plurality of ~~MCM's;~~ MCMs;

wire bonding each of the semiconductor devices of the plurality of semiconductor devices to its associated MCM;

testing each semiconductor device of the plurality of semiconductor devices on each MCM of the plurality of ~~MCM's~~ MCMs for opens and shorts;

encapsulating each semiconductor device of the plurality of semiconductor devices on each MCM of the plurality of ~~MCM's;~~ MCMs;

retesting each semiconductor device of the plurality of semiconductor devices on each MCM of the plurality of ~~MCM's~~ MCMs for opens and shorts;

burn-in testing each semiconductor device of the plurality of semiconductor devices on each MCM of the plurality of ~~MCM's;~~ MCMs;

back-end testing each semiconductor device of the plurality of semiconductor devices on each MCM of the plurality of ~~MCM's;~~ MCMs;

automatically reading the fuse identification of each semiconductor device of the plurality of semiconductor devices in each MCM of the plurality of ~~MCM's;~~ MCMs;

accessing the data stored in association with the fuse identification of each semiconductor device of the plurality of semiconductor devices;

for any semiconductor device of the plurality of semiconductor devices failing any one of the opens/shorts, burn-in, and back-end tests, evaluating the accessed data to determine whether the failing semiconductor device may be repaired;

repairing any semiconductor device of the plurality of semiconductor devices determined in accordance with the accessed data to be repairable and returning repaired ~~MCM's~~ MCMs to the manufacturing process; and

replacing any semiconductor device of the plurality of semiconductor devices determined in accordance with the accessed data to be unrepairable with a Known Good Die (KGD) and returning the repaired ~~MCM's~~ MCMs to the manufacturing process.

32. (Currently amended) The method of claim 31, further comprising plasma cleaning each MCM of the plurality of ~~MCM's~~ MCMs after curing the epoxy on the bonding sites of each MCM.

33. (Currently amended) The method of claim 31, wherein mounting the semiconductor wafers comprises mounting each semiconductor wafer of the plurality of semiconductor wafers on an Ultraviolet (U.V.) adhesive film, wherein the method further comprises exposing the U.V. adhesive film to U.V. light to loosen each semiconductor wafer of the ~~wafer~~ plurality of semiconductor wafers from the film prior to picking and placing each semiconductor device of the plurality of semiconductor devices.

34. (Currently amended) The method of claim 31, further comprising singulating the printed circuit boards associated with each MCM of the plurality of ~~MCM's.~~ MCMs.

35. (Currently amended) A method of manufacturing Multi-Chip Modules ~~(MCM's)~~ (MCMs) from semiconductor wafers using flip-chip techniques, the method comprising:

providing a plurality of semiconductor wafers;

fabricating a plurality of semiconductor devices on each semiconductor wafer of the plurality of semiconductor wafers;

electronically probing each semiconductor device of the semiconductor devices on each semiconductor wafer of the plurality of semiconductor wafers to identify good, bad and repairable semiconductor devices on each semiconductor wafer of the plurality of semiconductor wafers;

repairing the repairable semiconductor devices;

programming each semiconductor device of the semiconductor devices on each semiconductor wafer of the plurality of semiconductor wafers to store a unique fuse identification;

storing an electronic wafer map for each semiconductor wafer of the plurality of semiconductor wafers that identifies locations of good and bad semiconductor devices on each semiconductor wafer and associates each semiconductor device on each semiconductor wafer with its fuse identification;

storing data in association with the fuse identification of each semiconductor device of the semiconductor devices identifying repairs performed on each semiconductor device of the semiconductor devices;

mounting each semiconductor wafer of the plurality of semiconductor wafers on an adhesive film;

sawing each semiconductor device of the semiconductor devices on each semiconductor wafer of the plurality of semiconductor wafers from its wafer to form a semiconductor device;

accessing the stored wafer map for each semiconductor wafer of the plurality of semiconductor wafers;

accessing the stored data for each semiconductor device of the semiconductor devices on each of the semiconductor wafers of the plurality of semiconductor wafers;

automatically picking each semiconductor device of the good semiconductor devices from its wafer;

discarding non-picked semiconductor devices identified as bad by the accessed wafer maps;

diverting picked semiconductor devices identified as good but unrepairable by the accessed wafer maps and data to a non-MCM device manufacturing process;

flip-chip attaching picked semiconductor devices identified as good and repairable by the accessed wafer maps and data to bonding sites of each printed circuit board of a plurality of printed circuit boards to form a plurality of ~~MCM's;~~ MCMs;

curing each MCM of the plurality of ~~MCM's;~~ MCMs;

testing each semiconductor device of the semiconductor devices on each MCM of the plurality of ~~MCM's~~ MCMs for opens and shorts;

encapsulating each semiconductor device of the semiconductor devices on each MCM of the plurality of ~~MCM's;~~ MCMs;

retesting each semiconductor device of the semiconductor devices on each MCM of the plurality of ~~MCM's~~ MCMs for opens and shorts;

burn-in testing each semiconductor device of the semiconductor devices on each MCM of the plurality ~~MCM's;~~ MCMs;

back-end testing each semiconductor device of the semiconductor devices on each MCM of the plurality of ~~MCM's;~~ MCMs;

automatically reading the fuse identification of each semiconductor device of the semiconductor devices in each MCM of the plurality of ~~MCM's;~~ MCMs;

accessing the data stored in association with the fuse identification of each semiconductor device of the semiconductor devices in each MCM of the plurality of ~~MCM's;~~ MCMs;

for any semiconductor device of the semiconductor devices on each MCM of the plurality failing any one of the opens/shorts, burn-in, and back-end tests, evaluating the accessed data to determine whether the failing semiconductor devices may be repaired;

repairing any semiconductor device of the semiconductor devices determined in accordance with the accessed data to be repairable and returning repaired ~~MCM's~~ MCMs to the manufacturing process; and

replacing any semiconductor device of the semiconductor devices determined in accordance with the accessed data to be unrepairable with a Known Good Die (KGD) and returning the repaired ~~MCM's~~ MCMs to the manufacturing process.

36. (Currently amended) The method of claim 35, wherein mounting the semiconductor wafers comprises mounting each semiconductor wafer of the plurality of semiconductor wafers on an Ultraviolet (U.V.) adhesive film, wherein the method further comprises exposing the U.V. adhesive film to U.V. light to loosen ~~the~~ each semiconductor wafer of the plurality of semiconductor wafers from the film prior to picking and flip-chip attaching each semiconductor device.

37. (Currently amended) The method of claim 35, further comprising singulating the printed circuit boards associated with each MCM of the plurality of ~~MCM's.~~ MCMs.

38. (Previously presented) A method in an integrated circuit semiconductor device in a Multi-Chip Module (MCM) manufacturing process for diverting good but unrepairable semiconductor devices from the process, the semiconductor devices being of the type to have a substantially unique identification code, the method comprising:

storing data in association with the identification code of each semiconductor device of the semiconductor devices identifying semiconductor devices that are good and repairable, that are good but unrepairable, and that are bad;

automatically reading the identification code of each semiconductor device of the semiconductor devices;

accessing the data stored in association with the identification code of each semiconductor device of the semiconductor devices;

diverting semiconductor devices identified as good but unrepairable by the accessed data to one of use in other semiconductor device manufacturing processes and discarding the semiconductor devices identified as good but unrepairable; and

discarding semiconductor devices identified as bad by the accessed data.

39. (Original) The method of claim 38, further comprising:

assembling at least one semiconductor device identified as good and repairable into at least one MCM.

40. (Previously presented) A semiconductor device manufacturing process using data related to manufacturing procedures used previously that a plurality of integrated circuits of semiconductor devices have undergone for selecting manufacturing procedures the plurality of integrated circuits of the semiconductor devices are to undergo during manufacture, each semiconductor device having integrated circuits and having a substantially unique identification code, the manufacturing process comprising:

storing data in association with the identification code of each semiconductor device of the semiconductor devices identifying manufacturing procedures the semiconductor device has undergone, said storing data comprising storing data that identifies repairs performed on each semiconductor device;

automatically reading the identification code of each semiconductor device; and

accessing the data stored in association with the identification code of each semiconductor device.

41. (Previously presented) The process of claim 40, further comprising:

selecting manufacturing procedures each semiconductor device undergoes in accordance with the accessed data.

42. (Cancelled)

43. (Currently amended) The process of claim 40 , wherein each semiconductor device ~~comprises~~ comprises a Dynamic Random Access Memory (DRAM) semiconductor device, wherein storing data comprises storing data that identifies spare rows and columns used in repairing each DRAM semiconductor device.

44. (Cancelled)

45. (Previously presented) The process of claim 40, wherein storing data comprises storing data at probe.

46. (Previously presented) The process of claim 40, wherein automatically reading the identification code of each semiconductor device comprises electrically retrieving a unique fuse ID programmed into each semiconductor device.

47. (Previously presented) The process of claim 40, wherein the identification code of each semiconductor device comprises an identification code including one of a fuse ID, dot code, and bar code.

48. (Previously presented) The process of claim 40, wherein the identification code of each semiconductor device comprises a dot code.

49. (Previously presented) The process of claim 40, wherein the identification code of each semiconductor device comprises an identification code including a bar code.

50. (Previously presented) The process of claim 40, wherein automatically reading the identification code of each semiconductor device comprises optically reading a unique ID code provided on each semiconductor device.

51. (Previously presented) The process of claim 50, wherein optically reading a unique ID code provided on each semiconductor device comprises optically reading a unique laser fuse ID programmed into each semiconductor device.

52. (Previously presented) The process of claim 40, wherein automatically reading the identification code of each semiconductor device comprises automatically reading the identification code of each semiconductor device at one of an opens/shorts test, a burn-in test, and a back-end test in the semiconductor device manufacturing process.

53. (Previously presented) The process of claim 40, wherein accessing the data stored in association with the identification code of each semiconductor device comprises accessing the data stored in association with the identification code of each semiconductor device at one of an opens/shorts test, a burn-in test, and a back-end test in the semiconductor device manufacturing process.

54. (Previously presented) The process of claim 41, wherein selecting the manufacturing procedures each semiconductor device undergoes in accordance with the accessed data comprises selecting repairs each semiconductor device undergoes in accordance with the accessed data.

55. (Previously presented) The process of claim 54, wherein each semiconductor device comprises a Dynamic Random Access Memory (DRAM) semiconductor device, and wherein selecting repairs each semiconductor device undergoes comprises selecting spare rows and columns used to repair the DRAM semiconductor device.

56. (Previously presented) The process of claim 41, wherein selecting manufacturing procedures each semiconductor device undergoes in accordance with the accessed data comprises selecting whether each semiconductor device undergoes repair procedures.

57. (Previously presented) The process of claim 56, wherein each semiconductor device comprises a Dynamic Random Access Memory (DRAM) semiconductor device, and wherein selecting whether each semiconductor device undergoes repair procedures comprises selecting whether each DRAM semiconductor device will be repaired in accordance with whether the accessed data indicates enough spare rows and columns are available in each semiconductor device to effect repairs.

58. (Currently amended) The process of claim 41, wherein selecting manufacturing procedures each semiconductor device will undergo in accordance with the accessed data comprises determining whether each semiconductor device will be assembled into Multi-Chip Modules ~~(MCM's)~~ (MCMs) in accordance with whether the accessed data indicates each semiconductor device is repairable.

59. (Currently amended) The process of claim 40, further comprising assembling each semiconductor device into a packaged semiconductor device after ~~the step of~~ storing data and before ~~the step of~~ automatically reading the identification code of each semiconductor device.

60. (Currently amended) A method of manufacturing semiconductor devices from wafers, the method comprising:

providing a plurality of wafers;

fabricating a plurality of semiconductor devices on at least one wafer of the plurality of wafers;

causing each semiconductor device of the plurality on the at least one wafer of the plurality of wafers to store a substantially unique identification code, said causing each of the semiconductor devices to store a substantially unique identification code comprising applying a dot code to each of the semiconductor devices;

storing data in association with the identification code of each semiconductor device that identifies manufacturing procedures each semiconductor device has undergone, said storing data comprising storing data that identifies rows and columns used in manufacturing procedures for repairing a semiconductor device;

separating each semiconductor device on the at least one wafer of the plurality of wafers from the at least one wafer of the plurality of wafers to form at least one semiconductor device;

assembling the at least one semiconductor device into a semiconductor device assembly;

automatically reading the identification code associated with the at least one semiconductor device; and

accessing the data stored in association with the identification code associated with the at least one semiconductor device.

61. (Original) The method of claim 60, further comprising:

selecting manufacturing procedures the at least one semiconductor device undergoes in accordance with the accessed data.

62. (Currently amended) The method of claim 60, wherein fabricating a plurality of semiconductor devices on at least one wafer of the plurality of wafers comprises fabricating semiconductor devices selected from a group comprising Dynamic Random Access Memory (DRAM) semiconductor devices, Static Random Access Memory (SRAM) semiconductor devices, Synchronous DRAM (SDRAM) semiconductor devices, processor semiconductor devices, Rambus in-line memory module type semiconductor devices, small outline Rambus in-line memory module type semiconductor devices, and personal computer memory format type semiconductor devices.

63. (Currently amended) The method of claim 60, wherein causing each of the semiconductor devices to store a substantially unique identification code comprises programming each semiconductor device on the at least one wafer of the plurality of wafers to permanently store a unique fuse ID.

64. (Cancelled)

65. (Previously presented) The method of claim 60, wherein causing each of the semiconductor devices to store a substantially unique identification code comprises applying a bar code to each of the semiconductor devices.

66. (Currently amended) The method of claim 63, wherein programming each semiconductor device on the at least one wafer of the plurality of wafers to permanently store a unique fuse ID code comprises programming at least one of fuses and anti-fuses in each semiconductor device on the at least one wafer of the plurality of wafers to permanently store the unique fuse ID.

67. (Currently amended) The method of claim 60, wherein assembling the at least one semiconductor device into a semiconductor device assembly comprises:

picking each of the plurality of semiconductor devices from the at least one wafer of the plurality of wafers;

placing each semiconductor device onto an epoxy-coated bonding site of one lead frame of a plurality of lead frames;

curing the epoxy on the bonding site of each lead frame of the plurality of lead frames;

wire bonding each semiconductor device to its associated lead frame;

encapsulating each semiconductor device and its associated lead frame to form one of a plurality of semiconductor device assembly packages, each package having projecting leads;

curing each of the semiconductor device assembly packages;

de-flashing the projecting leads of each semiconductor device assembly package;

electroplating the projecting leads of each semiconductor device assembly package; and

singulating each semiconductor device assembly package into one semiconductor device assembly package of a plurality of discrete semiconductor device assembly packages.

68. (Currently amended) The method of claim 60, wherein separating each semiconductor device on the at least one wafer of the plurality of wafers from the at least one wafer of the plurality of wafers to form at least one semiconductor device and wherein ~~the step of~~ assembling the at least one semiconductor device into a semiconductor device assembly comprise:

singulating at least one semiconductor device ~~of the plurality~~ from the at least one wafer of the plurality of wafers using a saw.

69. (Currently amended) The method of claim 60, wherein separating each semiconductor device on the at least one wafer of the plurality of wafers from the at least one wafer of the plurality of wafers to form at least one semiconductor device and wherein ~~the step of~~ assembling the at least one semiconductor device into a semiconductor device assembly comprise:

singulating at least one semiconductor device ~~of the plurality~~ from the at least one wafer of the plurality of wafers using a laser.

70. (Currently amended) The method of claim 60, wherein separating each semiconductor device on the at least one wafer of the plurality of wafers from the at least one wafer of the plurality of wafers to form at least one semiconductor device and wherein ~~the step of~~ assembling the at least one semiconductor device into a semiconductor device assembly comprises:

singulating at least one semiconductor device ~~of the plurality~~ from the at least one wafer of the plurality of wafers using a laser/water apparatus.

71. (Currently amended) The method of claim 60, wherein separating each semiconductor device on the at least one wafer of the plurality of wafers from the at least one wafer of the plurality of wafers to form at least one semiconductor device and wherein ~~the step of~~ assembling the at least one semiconductor device into a semiconductor device assembly comprises:

singulating at least one semiconductor device ~~of the plurality~~ from the at least one wafer of the plurality of wafers using a cool laser apparatus.

72. (Currently amended) The method of claim 60, wherein separating each semiconductor device on the at least one wafer of the plurality of wafers from the at least one wafer of the plurality of wafers to form at least one semiconductor device and wherein ~~the step of~~ assembling the at least one semiconductor device into a semiconductor device assembly comprises:

singulating at least one semiconductor device ~~of the plurality~~ from the at least one wafer of the plurality of wafers using a water jet apparatus.

73. (Previously presented) The method of claim 60, wherein assembling the at least one semiconductor device into a semiconductor device assembly comprises assembling the at least one semiconductor device into a semiconductor device assembly selected from a group comprising a wire bond/lead frame semiconductor device, a Chip-On-Board (COB) semiconductor device, a flip-chip semiconductor device, and a Board-Over-Chip (BOC) semiconductor device.

74. (Previously presented) The method of claim 60, wherein assembling the at least one semiconductor device into a semiconductor device assembly comprises:

mounting the at least one semiconductor device on one of a lead frame of a plurality of lead frames and a substrate;

encapsulating the at least one semiconductor device and a portion of the one of a lead frame and a substrate, forming a semiconductor device assembly package; and

singulating the semiconductor device assembly package from the one of a plurality of lead frames and a substrate to form one semiconductor device assembly package.

75. (Previously presented) The method of claim 74, wherein singulating the semiconductor device assembly package from the one of a plurality of lead frames and a substrate to form one semiconductor device assembly package comprises the use of a saw.

76. (Previously presented) The method of claim 74, wherein singulating the semiconductor device assembly package from the one of a plurality of lead frames and a substrate to form one semiconductor device assembly package comprises the use of a laser.

77. (Previously presented) The method of claim 74, wherein singulating the semiconductor device assembly package from the one of a plurality of lead frames and a substrate to form one semiconductor device assembly package comprises the use of a laser/water apparatus.

78. (Previously presented) The method of claim 74, wherein singulating the semiconductor device assembly package from the one of a plurality of lead frames and a substrate to form one semiconductor device assembly package comprises the use of a cool laser.

79. (Previously presented) The method of claim 74, wherein singulating the semiconductor device assembly package from the one of a plurality of lead frames and a substrate to form one semiconductor device assembly package comprises the use of a water jet.

80. (Currently amended) A method of manufacturing semiconductor devices from a plurality of wafers, the method comprising:

providing a plurality of wafers;

fabricating a plurality of semiconductor devices on at least one wafer of the plurality of wafers;

causing at least one semiconductor device of the plurality on the at least one wafer of the plurality of wafers to store a substantially unique identification code;

storing data in association with the identification code of the at least one semiconductor device identifying manufacturing procedures the at least one semiconductor device has undergone, said storing data comprising storing data that identifies repairs performed on each semiconductor device;

separating the at least one semiconductor device and at least one other semiconductor device on the at least one wafer of the plurality of wafers from the at least one wafer of the plurality of wafers to form at least two semiconductor devices on a portion of the at least one wafer of the plurality of wafers;

assembling the at least two semiconductor devices into a semiconductor device assembly;

automatically reading the identification code associated with the at least two semiconductor devices; and

accessing the data stored in association with the identification code associated with the at least two semiconductor devices.

81. (Original) The method of claim 80, further comprising:

selecting manufacturing procedures the at least one semiconductor device undergoes in accordance with the accessed data.

82. (Currently amended) The method of claim 80, wherein fabricating a plurality of semiconductor devices on at least one wafer of the plurality of wafers comprises fabricating semiconductor devices selected from a group comprising Dynamic Random Access Memory (DRAM) semiconductor devices, Static Random Access Memory (SRAM) semiconductor devices, Synchronous DRAM (SDRAM) semiconductor devices, processor semiconductor devices, Rambus in-line memory module type semiconductor devices, small outline Rambus in-line memory module type semiconductor devices, and personal computer memory format type semiconductor devices.

83. (Currently amended) The method of claim 80, wherein causing the at least one semiconductor device to store a substantially unique identification code comprises programming the at least one semiconductor device on the at least one wafer of the plurality of wafers to permanently store a unique fuse ID.

84. (Previously presented) The method of claim 80, wherein causing the at least one semiconductor device to store a substantially unique identification code comprises applying a dot code to the at least one semiconductor device.

85. (Previously presented) The method of claim 80, wherein causing the at least one semiconductor device to store a substantially unique identification code comprises applying a bar code to the at least one semiconductor device.

86. (Currently amended) The method of claim 83, wherein programming the at least one semiconductor device on the at least one wafer of the plurality of wafers to permanently store a unique fuse ID code comprises programming at least one of fuses and anti-fuses in the at least one semiconductor device on the at least one wafer of the plurality of wafers to permanently store the unique fuse ID.

87. (Currently amended) The method of claim 80, wherein assembling the at least two semiconductor devices into a semiconductor device assembly comprises:

picking the at least two semiconductor devices from the at least one wafer of the plurality of wafers;

placing the at least two semiconductor devices onto a bonding site of a substrate;

encapsulating at least one semiconductor device of the at least two semiconductor devices to form one of at least one semiconductor device assembly package; and

singulating the at least one semiconductor device assembly package.

88. (Currently amended) The method of claim 80, wherein separating the at least one semiconductor device and the at least one other semiconductor device on the at least one wafer from the at least one wafer of the plurality of wafers to form at least two semiconductor devices on a portion of the at least one wafer of the plurality of wafers comprises:
singulating the at least two semiconductor devices from the at least one wafer of the plurality of wafers using a saw.

89. (Currently amended) The method of claim 80, wherein separating the at least one semiconductor device and the at least one other semiconductor device on the at least one wafer from the at least one wafer of the plurality of wafers to form at least two semiconductor devices on a portion of the at least one wafer of the plurality of wafers comprises:
singulating the at least two semiconductor devices from the at least one wafer of the plurality of wafers using a laser.

90. (Currently amended) The method of claim 80, wherein separating the at least one semiconductor device and the at least one other semiconductor device on the at least one wafer from the at least one wafer of the plurality of wafers to form at least two semiconductor devices on a portion of the at least one wafer of the plurality of wafers comprises:
singulating the at least two semiconductor devices from the at least one wafer of the plurality of wafers using a laser/water apparatus.

91. (Currently amended) The method of claim 80, wherein separating the at least one semiconductor device and the at least one other semiconductor device on the at least one wafer from the at least one wafer of the plurality of wafers to form at least two semiconductor devices on a portion of the at least one wafer of the plurality of wafers comprises:
singulating the at least two semiconductor devices from the at least one wafer of the plurality of wafers using a cool laser apparatus.

92. (Currently amended) The method of claim 80, wherein separating the at least one semiconductor device and the at least one other semiconductor device on the at least one wafer from the at least one wafer of the plurality of wafers to form at least two semiconductor devices on a portion of the at least one wafer of the plurality of wafers comprises:
singulating the at least two semiconductor devices from the at least one wafer of the plurality of wafers using a water jet apparatus.

93. (Previously presented) The method of claim 80, wherein assembling the at least two semiconductor devices into a semiconductor device assembly comprises assembling the at least two semiconductor devices into a semiconductor device assembly selected from a group comprising a wire bond/lead frame semiconductor device, a Chip-On-Board (COB) semiconductor device, a flip-chip semiconductor device, and a Board-Over-Chip (BOC) semiconductor device.

94. (Original) The method of claim 80, wherein assembling the at least two semiconductor devices into a semiconductor device assembly comprises:
mounting the at least two semiconductor devices on a substrate;
encapsulating each semiconductor device and a portion of the substrate forming semiconductor device assembly packages; and
singulating the semiconductor device assembly packages.

95. (Previously presented) The method of claim 94, wherein singulating the semiconductor device assembly package comprises the use of a saw.

96. (Previously presented) The method of claim 94, wherein singulating the semiconductor device assembly package comprises the use of a laser.

97. (Previously presented) The method of claim 94, wherein singulating the semiconductor device assembly package comprises the use of a laser/water apparatus.

98. (Previously presented) The method of claim 94, wherein singulating the semiconductor device assembly package comprises the use of a cool laser.

99. (Previously presented) The method of claim 94, wherein singulating the semiconductor device assembly package comprises the use of a water jet.

100. (Currently amended) A method of manufacturing semiconductor devices from a plurality of wafers, the method comprising:

providing a plurality of wafers;

fabricating a plurality of semiconductor devices on at least one wafer of the plurality of wafers;

causing at least one semiconductor device of the plurality on the at least one wafer of the plurality of wafers to store a substantially unique identification code;

storing data in association with the identification code of the at least one semiconductor device identifying manufacturing procedures the at least one semiconductor device has undergone, said storing data comprising storing data that identifies repairs performed on each semiconductor device;

assembling the at least one wafer of the plurality of wafers into a semiconductor device assembly;

automatically reading the identification code associated with the at least one semiconductor device; and

accessing the data stored in association with the identification code associated with the at least one semiconductor device.

101. (Original) The method of claim 100, further comprising:
selecting manufacturing procedures the at least one semiconductor device undergoes in accordance with the accessed data.

102. (Currently amended) The method of claim 100, wherein fabricating a plurality of semiconductor devices on at least one wafer of the plurality of wafers comprises fabricating semiconductor devices selected from a group comprising Dynamic Random Access Memory (DRAM) semiconductor devices, Static Random Access Memory (SRAM) semiconductor devices, Synchronous DRAM (SDRAM) semiconductor devices, processor semiconductor devices, Rambus in-line memory module type semiconductor devices, small outline Rambus in-line memory module type semiconductor devices, and personal computer memory format type semiconductor devices.

103. (Currently amended) The method of claim 100, wherein causing the at least one semiconductor device to store a substantially unique identification code comprises programming the at least one semiconductor device on the at least one wafer of the plurality of wafers to permanently store a unique fuse ID.

104. (Previously presented) The method of claim 100, wherein causing the at least one semiconductor device to store a substantially unique identification code comprises applying a dot code to the at least one semiconductor device.

105. (Previously presented) The method of claim 100, wherein causing the at least one semiconductor device to store a substantially unique identification code comprises applying a bar code to the at least one semiconductor device.

106. (Currently amended) The method of claim 103, wherein programming the at least one semiconductor device on the at least one wafer of the plurality of wafers to permanently store a unique fuse ID comprises programming at least one of fuses and anti-fuses in the at least one semiconductor device on the at least one wafer of the plurality of wafers to permanently store the unique fuse ID.

107. (Currently amended) The method of claim 100, wherein assembling the at least one wafer of the plurality of wafers into a semiconductor device assembly comprises assembling the at least one wafer of the plurality of wafers into a semiconductor device assembly selected from a group comprising a Chip-On-Board (COB) semiconductor device, a flip-chip semiconductor device, and a Board-Over-Chip (BOC) semiconductor device.

108. (Currently amended) The method of claim 100, wherein assembling the at least one wafer of the plurality of wafers into a semiconductor device assembly comprises:

mounting the at least one wafer of the plurality of wafers on a substrate; and

encapsulating the at least one wafer of the plurality of wafers and a portion of the substrate, forming a wafer scale semiconductor device assembly package.